

MRAM concepts for extended scalability and ultrafast switching

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About me



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Thermally assisted MRAM

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form 17 November 2006

1919165218

es (MRAMs) are a new non-volatile memory if as a mainstream technology. MRAM cell ed writing scheme (TA-MRAM) is described design challenges. This approach is compared thine the improvements in write selectivity.

United States
(12) Patent Application Publication (19) Pub. No.: US 2005/0062228 A1
Dieny et al. (19) Pub. Date: Jan. 6, 2005

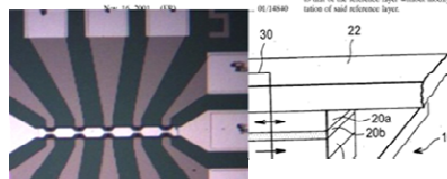
(54) MAGNETIC DEVICE WITH MAGNETIC TUNNEL JUNCTION, MEMORY ARRAY AND READ/WRITE METHODS USING SAME
(51) Int. Cl.⁷ G11C 11/14
(52) U.S. Cl. 365/171
(57) ABSTRACT

Publication Classification
(51) Int. Cl.⁷ G11C 11/14
(52) U.S. Cl. 365/171
(57) ABSTRACT

Magnetic tunnel junction magnetic device, memory and writing, and reading, methods using said device.
Said device (10) comprises a reference layer (20a) and a storage layer (20b) separated by a semiconductor or insulating layer (20c). The blocking temperature of the magnetization of the storage layer is lower than that of the reference layer. The device further comprises means (22, 24) for heating the storage layer above the blocking temperature of its magnetization and means (24) for applying to it a magnetic field (24) orientating its magnetization in relation to that of the reference layer without modifying the orientation of said reference layer.

Correspondence Address:
Thierry Dieny, A. Priot
PO Box 54640
San Jose, CA 95164-0640 (US)

(21) Appl. No.: 10/495,637
(22) PCT Filed: Nov. 16, 2002
(60) PCT No.: PCT/FR02/03096
(70) Foreign Application Priority Data
Nov. 16, 2001 (FR) 01/14040



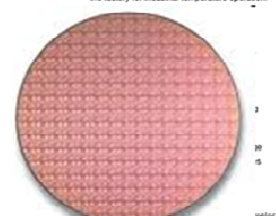
PRELIMINARY

CTMR01A08
128K x 8 MRAM Memory

General Description

The Crocus Technology CTMR01A08 is a 1Mbit Magnetic Random Access Memory (MRAM) device organized as 131,072 words by 8 bits. The CTMR01A08 offers SRAM compatible 30ns read/write timing with unlimited endurance. Data is always non-volatile, with data retention greater than 20 years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltages out of specification. The CTMR01A08 is the ideal low power solution for data logging, program store, data buffering and data cache applications.

The CTMR01A08 is available in 32-pin SOIC plastic packages and 48-pin SSOP packages. These packages are compatible with similar low-power SRAM products and other non-volatile RAM products. Crocus Technology memory devices provide highly reliable data storage over a wide range of operating temperatures. The product is offered for commercial temperature (0 to +70°C) operation. Please consult the factory for industrial temperature operation.



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A ₇	A ₈	A ₉	A ₁₀	A ₁₁	A ₁₂	A ₁₃	A ₁₄	A ₁₅	A ₁₆	A ₁₇	A ₁₈	A ₁₉	A ₂₀	A ₂₁	A ₂₂	A ₂₃	A ₂₄	A ₂₅	A ₂₆	A ₂₇	A ₂₈	A ₂₉	A ₃₀
Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	Q ₈	Q ₉	Q ₁₀	Q ₁₁	Q ₁₂	Q ₁₃	Q ₁₄	Q ₁₅	Q ₁₆	Q ₁₇	Q ₁₈	Q ₁₉	Q ₂₀	Q ₂₁	Q ₂₂	Q ₂₃	Q ₂₄	Q ₂₅	Q ₂₆	Q ₂₇	Q ₂₈	Q ₂₉



Prix SEE-IEEE
Leon-Nicolas Brillouin
2012

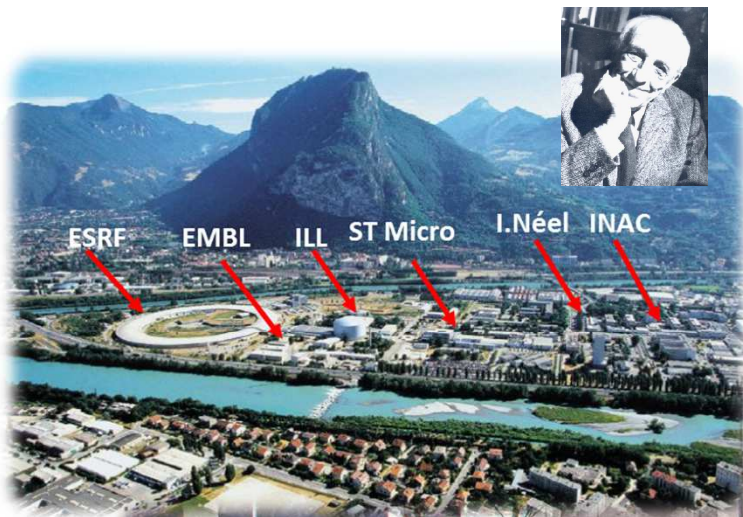
NEXT EU FP6 project (2002-2006)
finalist Descartes Prize in 2006



ANVAR Grand prize for innovation (2005)
13.5 Million Euros raised from VCs (2006)

Forum Romanians in Micro- and Nanoelectronics, 6 November 2018, Romanian Academy, Bucharest, Romania

About SPINTEC



Created in 2002, now - about 95-100 staff
40 permanent staff & 50-60 PhDs , post-docs & visitors

Forum Romanians in Micro- and Nanoelectronics, 6 November 2018, Romanian Academy, Bucharest, Romania

Summary

Basics of spintronics

Success story: data storage

MRAM in microelectronics

Need for a non-volatile memory

MRAM roadmap

What's next?

Basics of spintronics

Electronics
Electron Charge

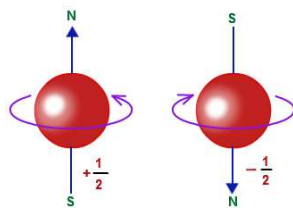


Peter Grunberg & Albert Fert

2007
Nobel Prize

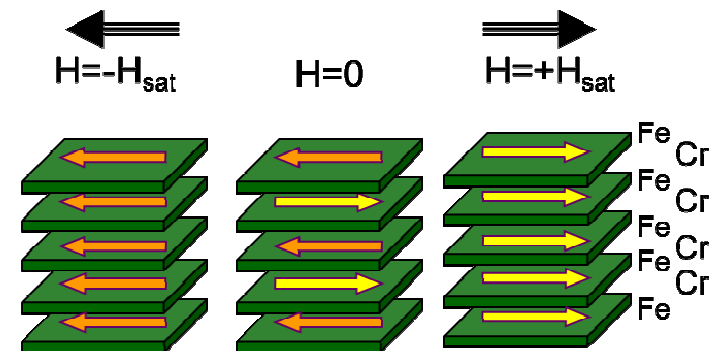
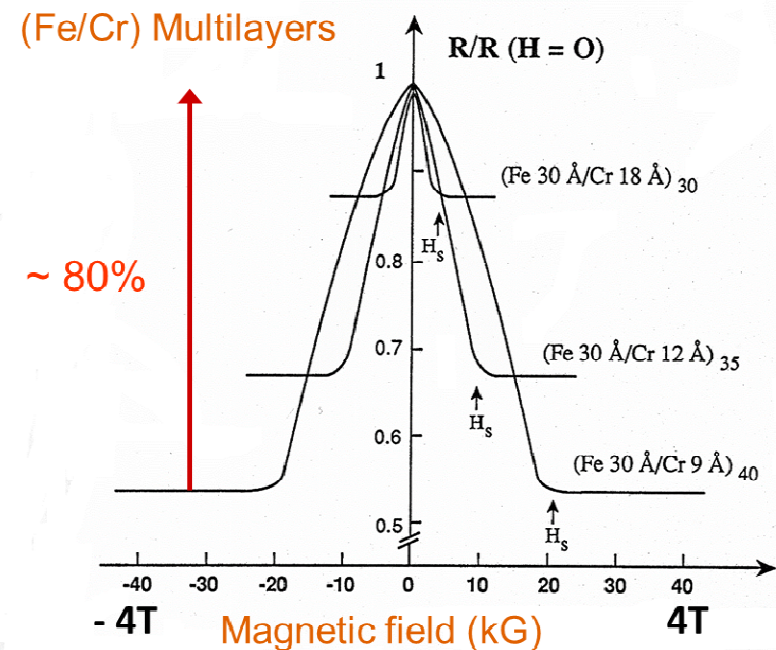


Magnetism
Electron Spin



Main goal of this hybrid technology:

Get the best of the two worlds to obtain new functionalities or
improve performances of electronics circuits

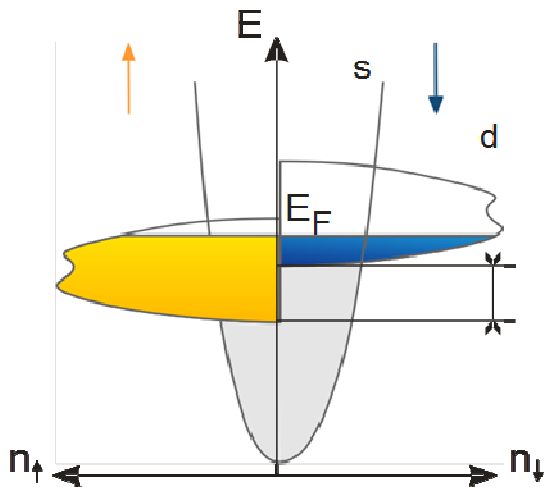


A. Fert et al, PRL (1988)

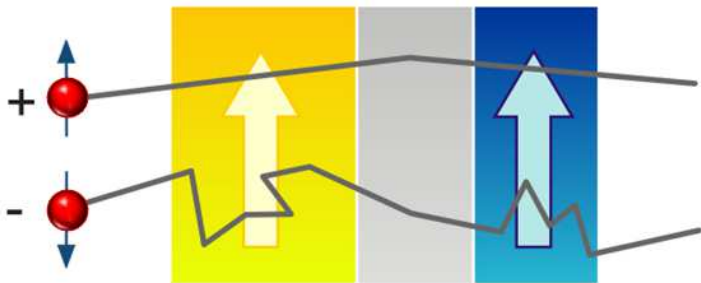
P. Grunberg et al, patent (1988) + PRB (1989)

Basics of spintronics

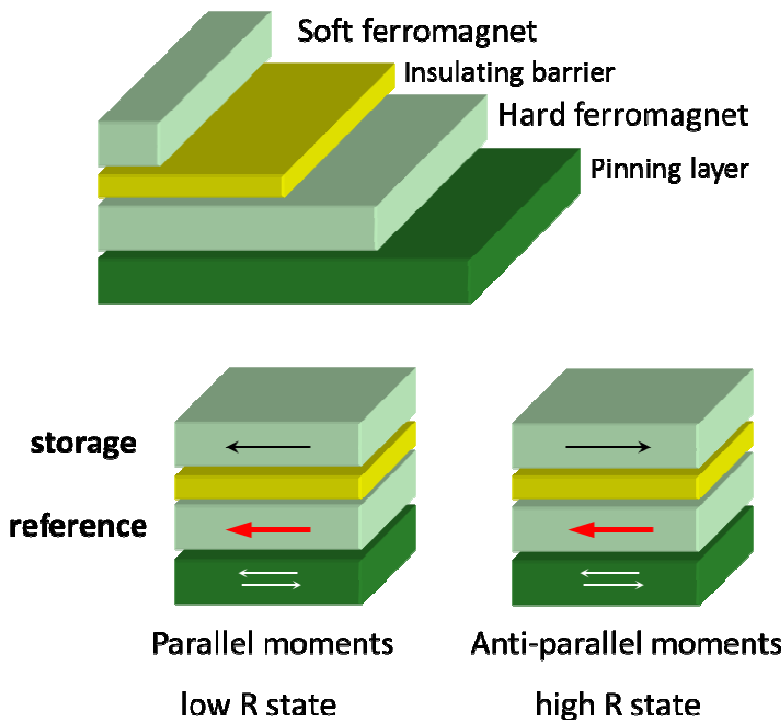
Spin dependent diffusion



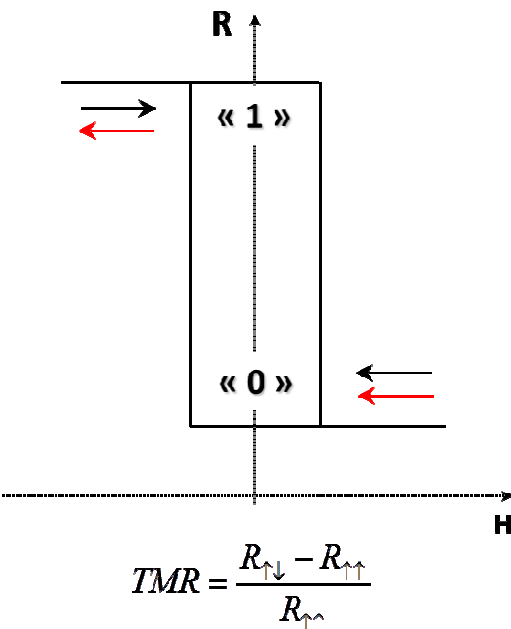
Magnetic hererostructures



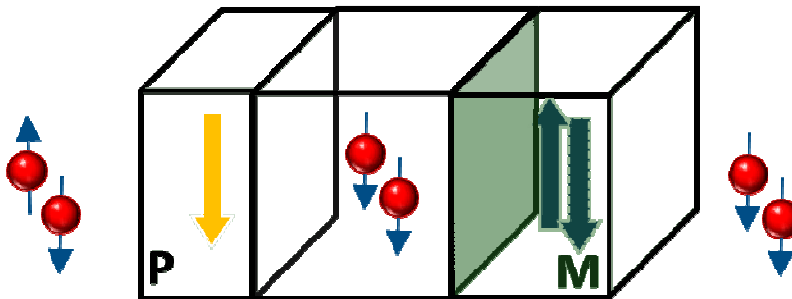
Magnetic tunnel junction, Spin valve



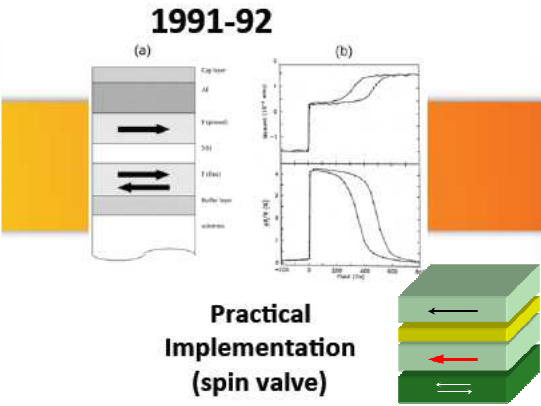
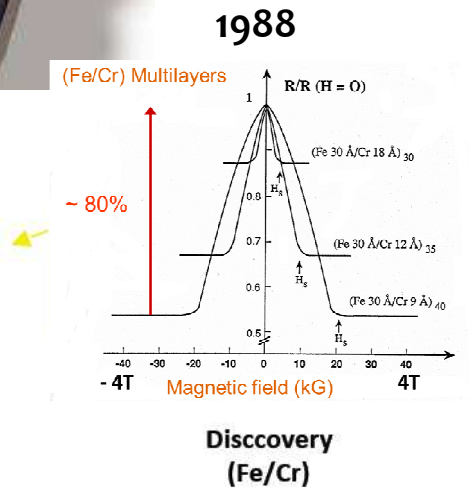
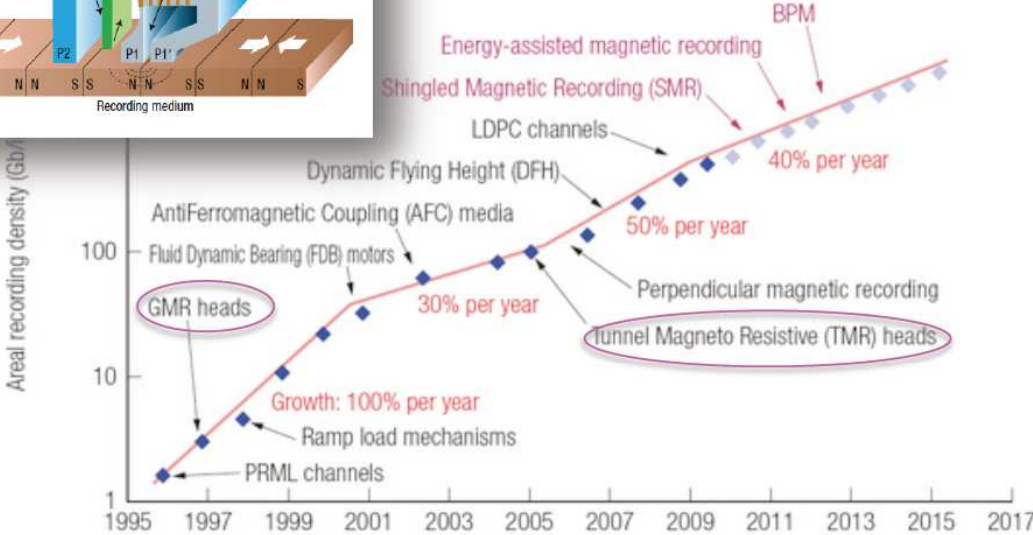
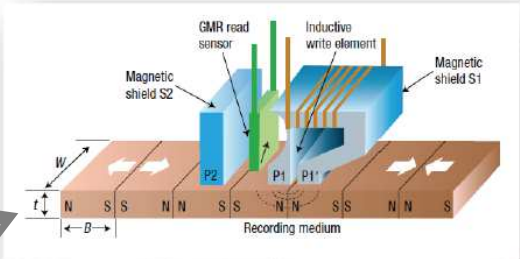
Magnetoresistance



Spin transfer torque



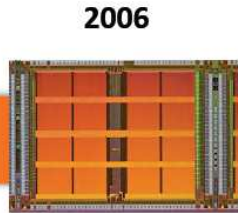
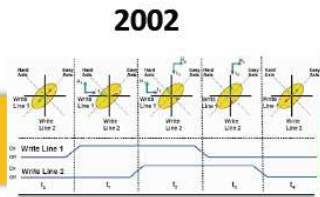
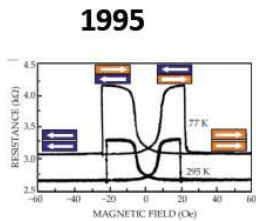
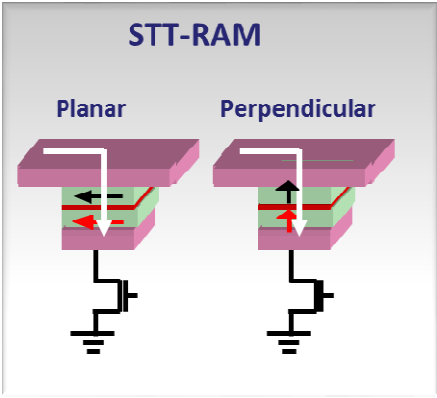
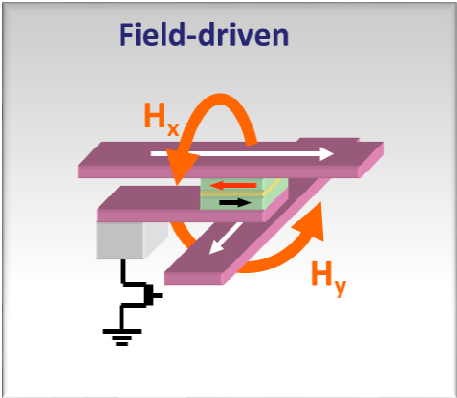
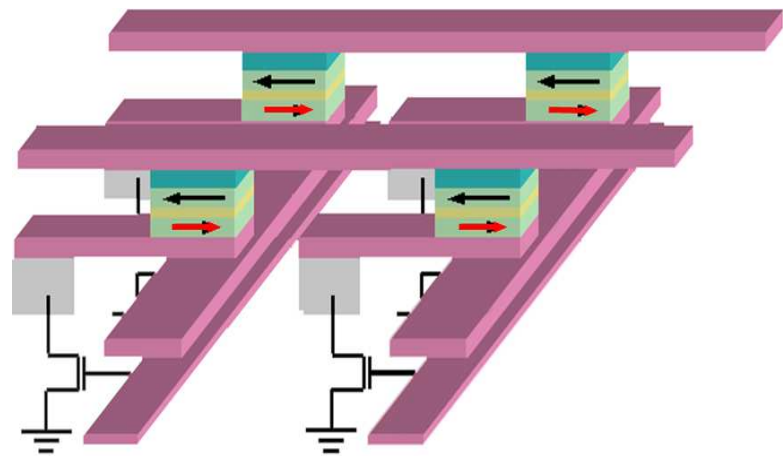
Success story : data storage



MRAM in microelectronics

For portable devices and « instant on » computing, industry needs a universal memory, that combine together low cost, low power, non volatility and speed.

S.Lai, Intel VP Technology

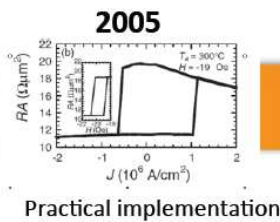


Toggle
MRAM

1996

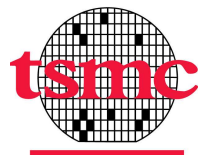
$$\mathbf{T} = \frac{1}{\Omega} \int_{\Omega} d\Omega \left(-\nabla \cdot \mathbf{J} - \frac{1}{\tau_{sf}} \mathbf{m} \right)$$

Theoretical prediction



STT
MRAM

MRAM in microelectronics



TSMC to start eMRAM production in 2018

Jun 08, 2017 **MRAM production**

According to reports, Taiwan Semiconductor Manufacturing Company (TSMC) is aiming to start producing embedded MRAM chips in 2018 using a 22 nm process. This will be initial "risk production" to gauge market reception.



DIGITIMES

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Samsung ready to mass produce MRAM chips using 28nm FD-SOI process

Yiling Lin, Taipei; Jessie Shen, DIGITIMES [Tuesday 26 September 2017]

Samsung Foundry will soon be ready to enter mass production of magnetoresistive random-access memory (MRAM) chips built using 28nm fully depleted silicon-on-insulator (FD-SOI) process technology, according to Korea media reports.

Samsung is reportedly teaming up with NXP and has completed the tape-out of its 28nm FD-SOI embedded MRAM, which will be first applied to NXP's new low-power i.MX-series solution targeted at automotive, multimedia and display panel applications.

In related news, Synopsys announced recently its Design Platform has been fully certified for use on Samsung Foundry's 28nm FD-SOI process technology. A PDK and a comprehensive reference flow, compatible with Synopsys' Lynx Design System, containing scripts, design methodologies and best practices are now available.



GLOBALFOUNDRIES



GF-Everspin 2X nm eMRAM with superior data retention - VLSI Symposium

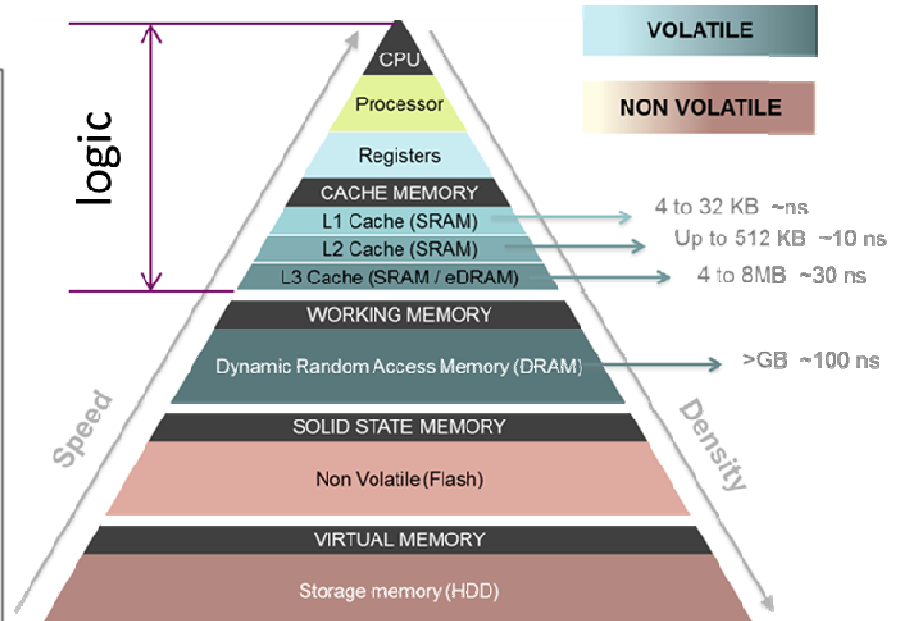
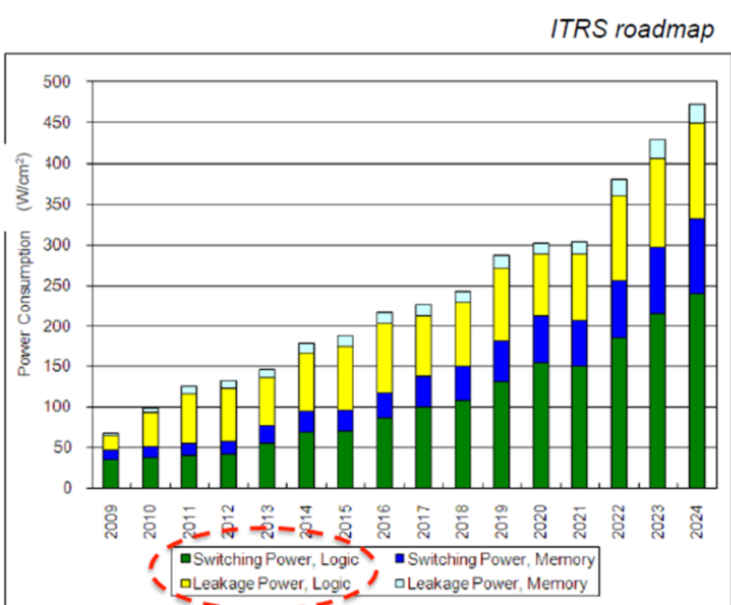
GLOBALFOUNDRIES and Everspin continue to drive embedded MRAM (eMRAM) forward into the 22nm process node! Please see our technical paper presented this week at VLSI Symposium in Japan.

For the first time, we are unveiling eMRAM that can retain data through solder reflow at 260C and 10+ years at 125C, plus read/write with outstanding endurance at 125C.

This is a major breakthrough from GLOBALFOUNDRIES and Everspin that enables eMRAM to be used for general purpose MCU's and Automotive SOCs.

Forum Romanians in Micro- and Nanoelectronics, 6 November 2018, Romanian Academy, Bucharest, Romania

Need for a non-volatile memory (low power & ultrafast)



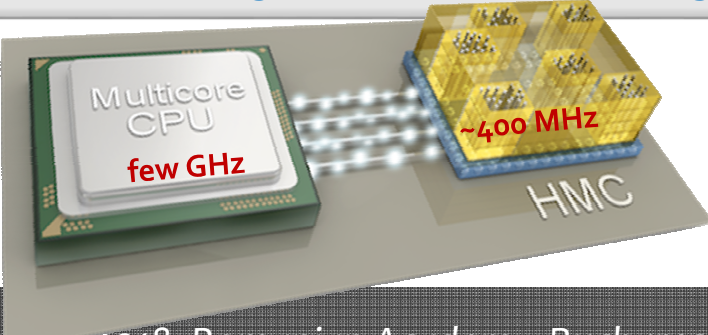
Bring non-volatility close to microprocessors

Need for ultrafast memories (sub-ns) directly integrated (process, design) at the heart of the logic

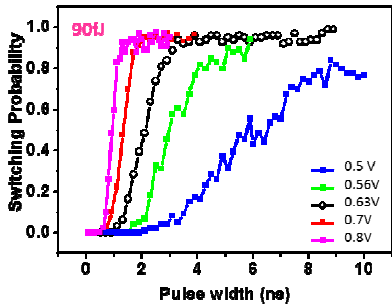
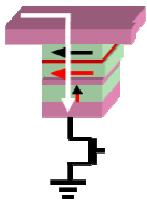
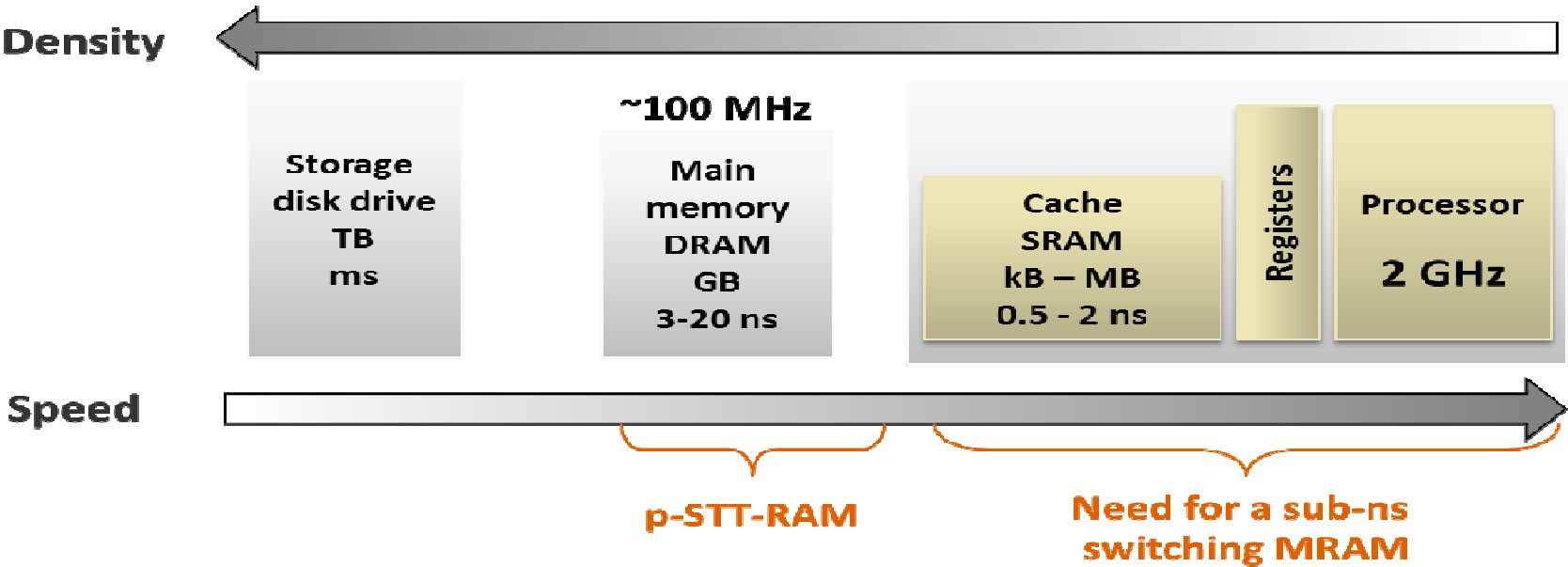
Memory vs. CPU speed mismatch

Logic keeps awaiting Data

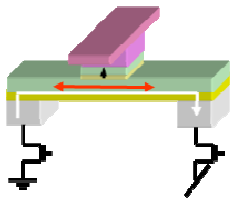
Logic issue is becoming a memory issue !



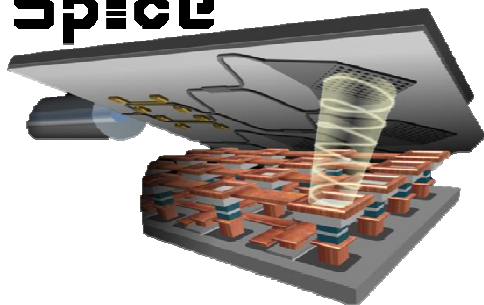
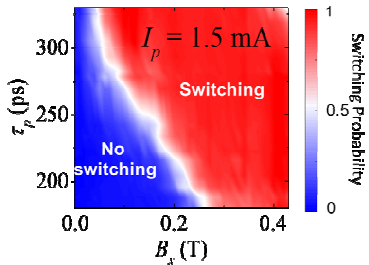
Need for a non-volatile memory (low power & ultrafast)



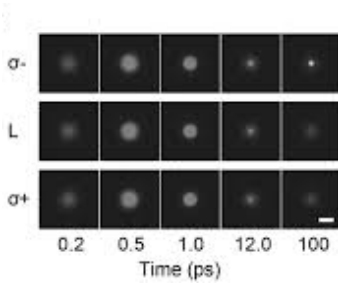
precesionnal



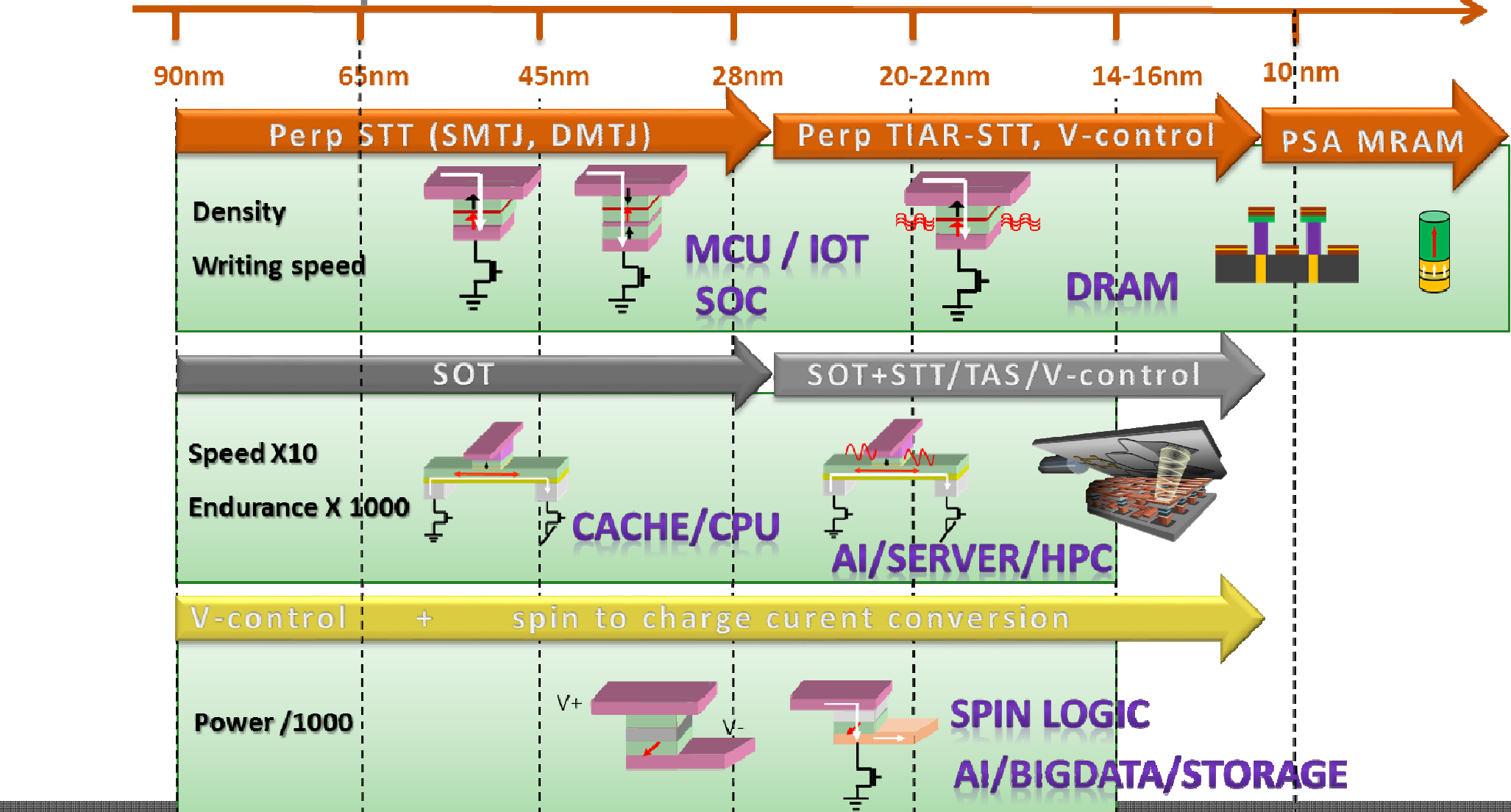
Spin Orbit Torque



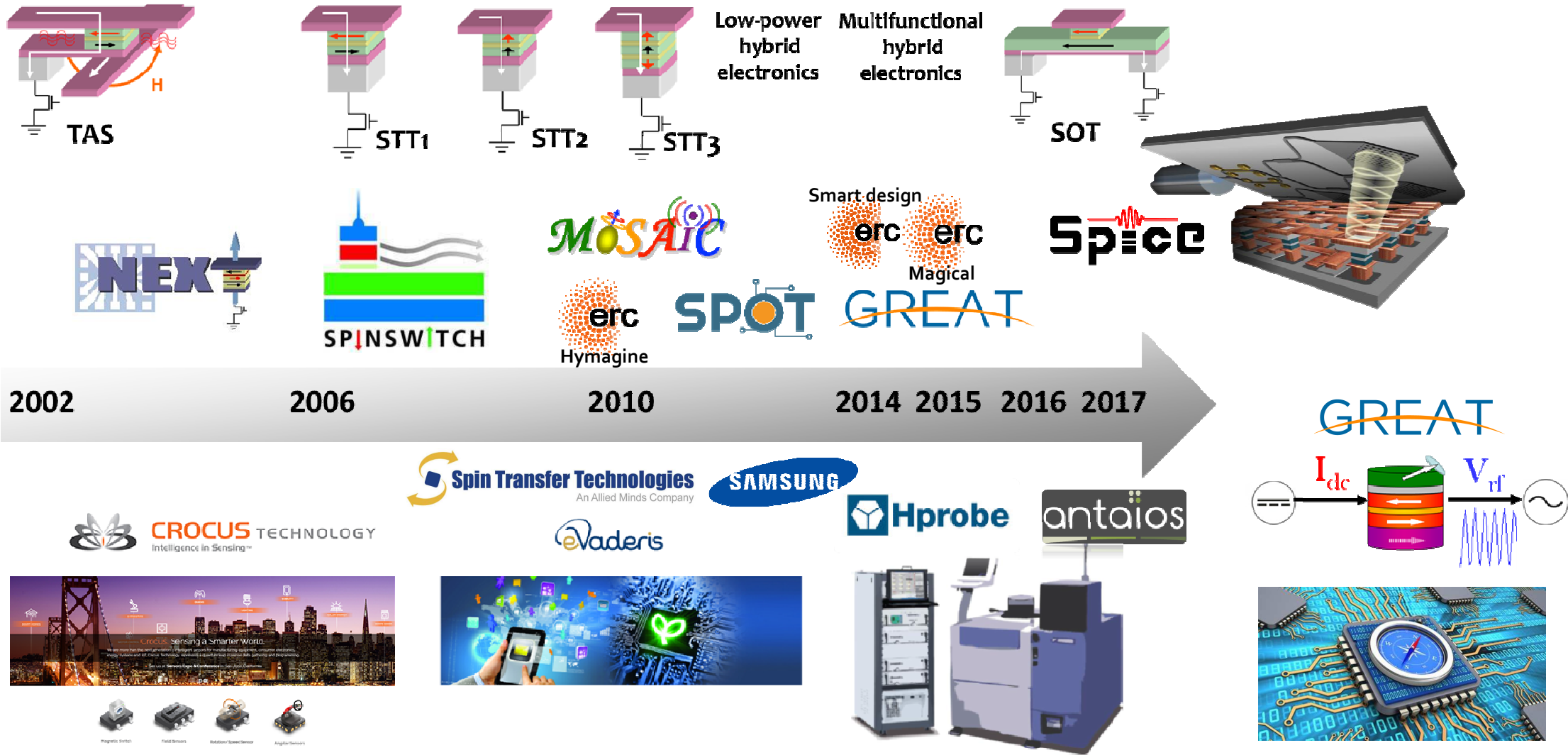
All optical switching



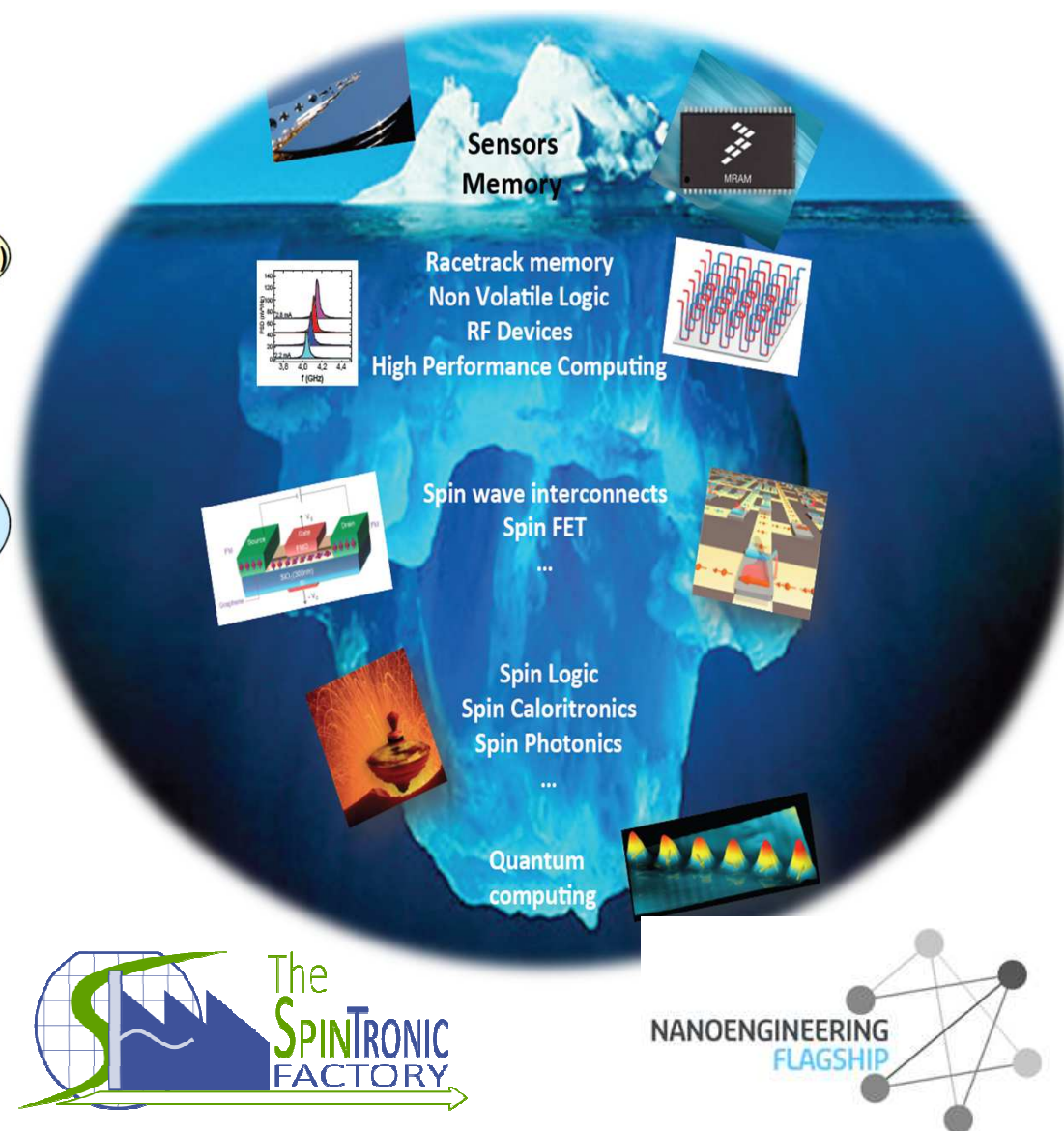
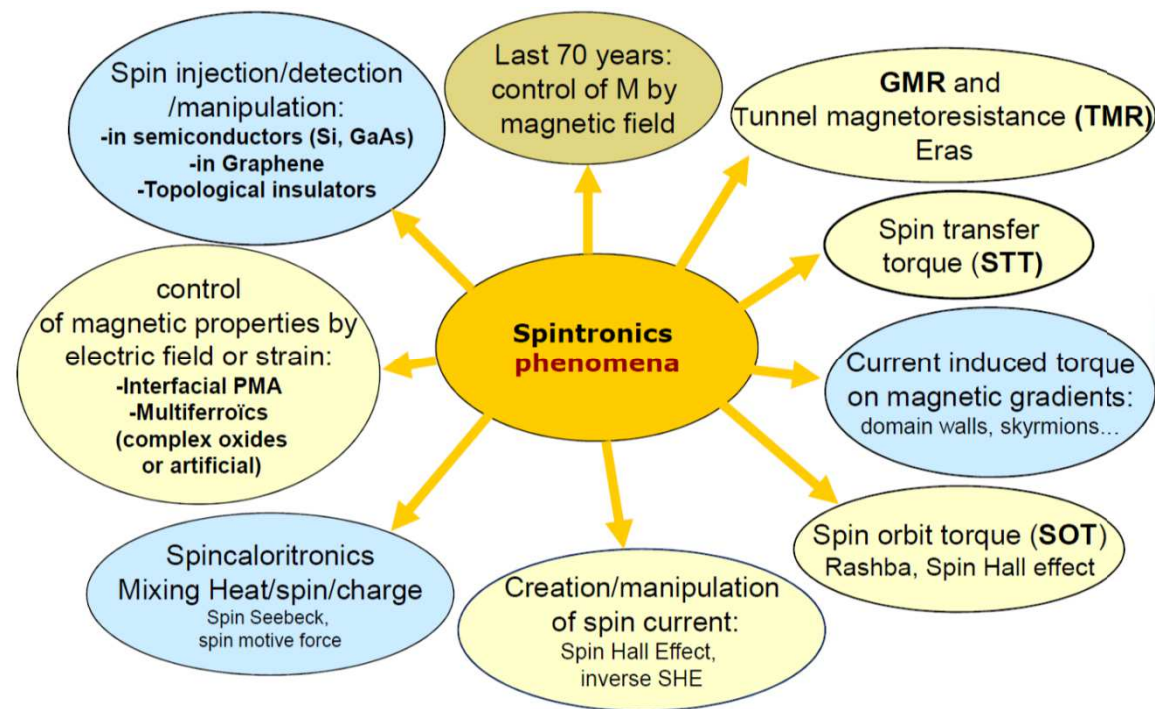
MRAM roadmap



MRAM @ SPINTEC



What's next?



FET Proactive TOCHA 2018-2023
Topological insulators

FET-OPEN NANOWAY 2019-2022
2D Materials

Forum Romanians in Micro- and Nanoelectronics, 6 November 2018, Romanian Academy, Bucharest, Romania



Thank you!

Lucian PREJBEANU

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www.spintec.fr